REMARKS

Claims 1-16 are pending in this application, of which claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 are being amended.

Claim Amendments

Claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 are being amended to further clarify the claim language. These amendments are supported at page 9, lines 31-33 of the Specification of the instant application. Furthermore, these amendments are not made for reasons related to patentability.

§102(b) Rejection of Claims 1-16 over Gilbert et al.

The Examiner rejected claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,805,861 to Gilbert et al. ("*Gilbert et al.*"). Applicants respectfully traverse the rejection for the following reasons.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim at issue must be found in the reference, either expressly described or under principles of inherency. Furthermore, "the elements must be arranged as required by the claim." M.P.E.P. § 2131. See also *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989).

Claim 1

Gilbert et al. fails to anticipate independent claim 1 for at least the reason that *Gilbert et al.* does not disclose a circuit designing apparatus comprising, inter alia, "**a logic verification unit configured to perform a logic verification by inputting a plurality of test vectors necessary for the logic verification to a circuit description**" and "**a test vector classifying unit configured to classify the test vectors into test vectors that pass through the changed logic cones and test vectors that do not pass through the changed logic cones, based on the profile information**," as recited in amended claim 1.

Instead, *Gilbert et al.* discloses "[a] method used by an electronic design automation system for stabilizing the names of components and nets of an integrated circuit from one design version to another" (Abstract). A Cone Graph Compare (CGC) module reads an old design and a new design from a Logic Design Database. The CGC module then "corrects the component and net names ... by analyzing the cones of logic contained in the design, comparing the old and new designs and assigning new names as needed. ... [T]he CGC module writes the name corrected design into the Logic Design Database" (Col. 11, line 62 to Col. 12, line 9).

Gilbert et al. does not disclose the "logic verification unit" and the "test vector classifying unit" for at least the reason that *Gilbert et al.* does not disclose the "plurality of test vectors" recited in claim 1. Neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description

to perform a logic verification, as required by claim 1. Also, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that "pass through" logic cones, as recited in amended claim 1. The test vectors inputted to the circuit description are used for "comparing an output signal and an expected value of the output signal, and judging the validity of the circuit description," as recited in claim 1. In contrast, the "user-defined names" and the "new names" of *Gilbert et al.* are "names." *Gilbert et al.* does not teach that these "names" can be inputted to a circuit description to perform a logic verification, or that these "names" can pass through logic cones. Thus, since neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute the "test vectors" recited in claim 1, *Gilbert et al.* does not teach the "logic verification unit" and the "test vector classifying unit" recited in claim 1.

Moreover, *Gilbert et al.* does not disclose the "logic verification unit" and the "test vector classifying unit" because *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 1. In reference to the "logic verification unit" recited in claim 1, the Examiner alleges that the "user-defined names" disclosed at Col. 11, lines 55-61, of *Gilbert et al.*, constitute the "test vectors" (Office Action, page 2). However, in reference to the "test vector classifying unit" recited in claim 1, the Examiner relies on the "new names" disclosed at Col. 12, lines 28-30, of *Gilbert et al.* (Office Action, page 3).

The "user-defined names" and the "new names" of *Gilbert et al.* are not the same names, in contrast to the "plurality of test vectors" inputted by the logic verification unit

of claim 1 and "the test vectors" classified by the test vector classifying unit of claim 1, which are the same test vectors. Instead, *Gilbert et al.* teaches that the "[n]ew component and net names are generated for the new logic design ..." (Col. 11, lines 17-18), whereas the "user-defined names" are "user-defined." Thus, since the "user-defined names" and the "new names" of *Gilbert et al.* are not arranged as required by claim 1, *Gilbert et al.* fails to teach the "logic verification unit" and the "test vector classifying unit" recited in claim 1.

Claim 3

Gilbert et al. also does not anticipate independent claim 3 for at least the reason that *Gilbert et al.* fails to disclose a circuit designing method comprising, inter alia, "**performing a logic verification by inputting a plurality of test vectors necessary for the logic verification to a circuit description defining a structure and a specification of a circuit to be designed and comparing an output signal and an expected value of the output signal, and judging the validity of the circuit description**" and "**classifying the test vectors into test vectors that pass through the changed logic cones and test vectors that do not pass through the changed logic cones, based on the profile information**," as recited in amended claim 3.

As explained above, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description in performing a logic verification, as required by claim 3. Also, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that "pass through"

logic cones, as recited in amended claim 3. Rather, the "user-defined names" and the "new names" of *Gilbert et al.* are "names". *Gilbert et al.* does not teach that these "names" can be inputted to a circuit description to perform a logic verification, or that these "names" can pass through logic cones.

Moreover, *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 3. In reference to "performing a logic verification," recited in claim 3, the Examiner alleges that the "user-defined names" disclosed at Col. 11, lines 55-61, of *Gilbert et al.*, constitute the "test vectors" (Office Action, page 2). However, in reference to "classifying the test vectors," recited in claim 3, the Examiner relies on the "new names" disclosed at Col. 12, lines 28-30, of *Gilbert et al.* (Office Action, page 3). The "user-defined names" and the "new names" of *Gilbert et al.* are not the same names, in contrast to the "plurality of test vectors" inputted in performing the logic verification of claim 3 and "the test vectors" classified in classifying the test vectors of claim 3, which are the same test vectors.

Claim 8

Additionally, *Gilbert et al.* fails to anticipate independent claim 8 for at least the reason that *Gilbert et al.* does not disclose a computer-readable recording medium storing a circuit designing program comprising and making a computer execute, inter alia, "**instructions configured to perform a logic verification by inputting a plurality of test vectors necessary for the logic verification into a circuit description defining a structure and a specification of a circuit to be designed and comparing**

an output signal and an expected value of the output signal, and judging the validity of the circuit description" and "**instructions configured to classify the test vectors into test vectors that pass through the changed logic cones and test vectors that do not pass through the changed logic cones, based on the profile information**," as recited in amended claim 8.

As explained above, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description to perform a logic verification, as required by claim 8. Also, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that "pass through" logic cones, as recited in amended claim 8. Rather, the "user-defined names" and the "new names" of *Gilbert et al.* are "names". *Gilbert et al.* does not teach that these "names" can be inputted to a circuit description to perform a logic verification, or that these "names" can pass through logic cones.

Moreover, *Gilbert et al.* does not disclose the "plurality of test vectors," arranged as required by claim 8. In reference to the "instructions configured to perform a logic verification" recited in claim 8, the Examiner alleges that the "user-defined names" disclosed at Col. 11, lines 55-61, of *Gilbert et al.*, constitute the "test vectors" (Office Action, page 2). However, in reference to the "instructions configured to classify the test vectors" recited in claim 8, the Examiner relies on the "new names" disclosed at Col. 12, lines 28-30, of *Gilbert et al.* (Office Action, page 3). The "user-defined names" and the "new names" of *Gilbert et al.* are not the same names, in contrast to the "plurality of test

vectors" inputted by the instructions configured to perform a logic verification of claim 8 and "the test vectors" classified by the instructions configured to classify the test vectors of claim 8, which are the same test vectors.

Thus, since *Gilbert et al.* does not teach each and every element of independent claims 1, 3, and 8, these claims should be allowed over *Gilbert et al.* under 35 U.S.C. § 102(b). Claims 2, 4-7, and 9-16 should also be allowed over *Gilbert et al.* under 35 U.S.C. § 102(b) for at least the reason that claims 2 and 12-14 depend from claim 1, claims 4-7 and 15 depend from claim 3, and claims 9-11 and 16 depend from claim 8.

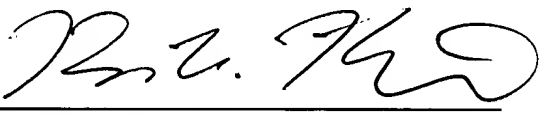
In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 1, 2005

By: 

Reece Nienstadt
Reg. No. 52,072

#956282